constant of 39.5. The single-section output matching network is formed in microstrip pattern on a 1-mm-thick alumina ceramic plate.

To obtain a basic understanding of circuit loss effects on low-impedance broad-band matching, matching circuit losses were analyzed and the results were presented.

The internally matched GaAs FET developed has a 2.5-W power output at 1-dB gain compression and a 4.4-W saturated power output with 5.5-dB linear gain from 4.2 to 7.2 GHz without external matching. The GaAs FET internally matched over the narrow band exhibited 5-W saturated power output with a linear gain of 6 dB from 4.5 to 6.5 GHz.

ACKNOWLEDGMENT

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Design Theory for Broad-Band YIG-Tuned FET Oscillators

ROBERT J. TREW, MEMBER, IEEE

***Abstract*—Design techniques that have been successfully used on the development of *X*-band GaAs FET YIG-tuned oscillators are presented. The design procedure results in the maximization of the oscillator bandwidth. Small-signal device characterization is utilized and accurately predicts the oscillator bandwidth. Spurious oscillation conditions are discussed, and design techniques are prescribed for eliminating spurious oscillations in both the active circuit and resonator. The operation of an experimental oscillator verifies the design procedure.**

I. INTRODUCTION

As GaAs FET technology matures circuit designers are looking to these devices for an increasing variety of applications. The high-frequency performance of FET's coupled with their high-efficiency potential make them attractive competitors to the more established solid-state components such as bulk-effect devices and bipolar transistors for use as fundamental signal sources.

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To date there have been relatively few reports in the literature on FET oscillator development. Most of the early reports were concerned with units characterized by relatively narrow bandwidths of a few percent [1]–[5]. More recent reports [6]–[8] establish the potential of the GaAs FET for use as broad-band fundamental signal sources but do not give detailed accounts of the design techniques used.

This paper presents circuit design techniques that have been used successfully in the design of *X*-band YIG-tuned oscillators. The design techniques result in maximization of the oscillator bandwidth. The circuit analysis also yields information on possible spurious oscillation conditions and their elimination. The operation of an experimental oscillator verifies the design predictions.

II. DESIGN TECHNIQUES

The design approach involves a computer model investigation of the interface between the device and feedback circuit and the microwave resonator, in this case a

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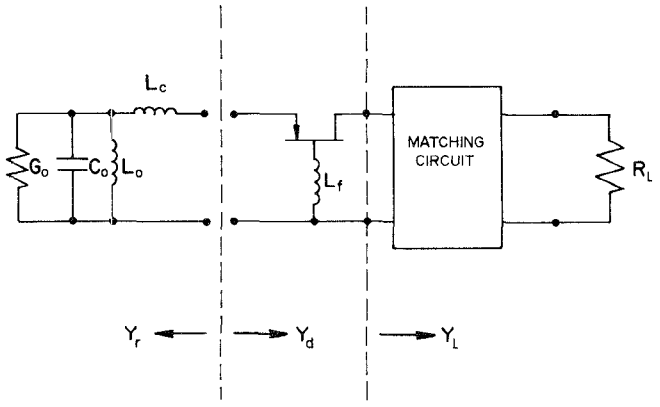

Fig. 1. YIG-tuned common-gate FET oscillator circuit.

YIG sphere and coupling loop (Fig. 1). For oscillations to occur, the sum of the admittances of the resonator and active circuit must equal zero [9]. The active circuit consists of the FET device and the feedback elements. Therefore,

$$Y_r + Y_d = 0 \tag{1}$$

or

$$G_r(\omega) - G_d(V_{\mathrm{RF}}, \omega) \leqslant 0 \tag{2}$$

and

$$B_r(\omega) + B_d(V_{\mathrm{RF}}, \omega) = 0. \tag{3}$$

Equation (2) establishes the potential for oscillations to occur. As the oscillations build up the active circuit conductance saturates with increasing RF voltage until steady state is achieved when the resonator and active circuit conductance are equal. The frequency of operation information is contained in (3). In addition to the conditions expressed in (2) and (3), stable oscillations are possible if and only if the stability criterion is satisfied [9]. That is

$$-V_{\mathrm{RF}} \frac{\partial G_d}{\partial V_{\mathrm{RF}}} \frac{dG_r}{d\omega} [\tan\theta + \tan\phi] > 0 \tag{4}$$

where

$$\tan\theta = \frac{dB_r}{d\omega} \Big/ \frac{dG_r}{d\omega}$$

and

$$\tan\phi = \frac{\partial B_d}{\partial V_{\mathrm{RF}}} \Big/ \frac{\partial G_d}{\partial V_{\mathrm{RF}}}.$$

Equations (2)–(4) comprise the necessary and sufficient criteria for steady-state oscillations.

The conditions expressed in (1)–(4) apply to both small- and large-signal operation. However, to apply these conditions to large-signal operation, it is necessary to know the quantitative dependence of Y_d upon RF voltage. This information is not easily obtained due to multifrequency effects at large RF voltages. For this work, experimentally determined small-signal S parameters are used to characterize the FET. The use of the small-signal characterization prevents the calculation of RF power and oscillator efficiency, but allows calculation of the theoretical tuning bandwidth since oscillations build up from small-signal conditions. In practice, good agreement is obtained between the theoretical and experimental tuning bandwidths. The agreement between the small-signal predictions and large-signal operation is consistent with the maximized bandwidth design that results in a reduced-peak negative conductance being generated by the device and feedback circuit. The oscillators produce approximately 10–20-mW RF power from devices that are capable of generating greater than 100 mW in narrow bandwidth applications. The relatively low-power operation of the FET's result in minimized saturation effects, and, therefore, good agreement between the theoretical and experimental results.

III. YIG Resonator

The equivalent circuit of the YIG resonator consists of a parallel resonant circuit in series with the coupling loop inductance (Fig. 1). The resonator input admittance [10] is given by

$$Y_r = 1/Z_r \tag{5}$$

with

$$Z_r = j\omega L_c + \frac{\left(\frac{j\omega\omega_0}{Q_u}\right)/G_0}{\omega_0^2 - \omega^2 + \left(\frac{j\omega\omega_0}{Q_u}\right)} \tag{6}$$

where

$$G_0 = 1/\mu_0 V K^2 \omega_M Q_u \tag{7}$$

$$L_0 = 1/G_0\omega_0 Q_u \tag{8}$$

and

$$C_0 = 1/L_0\omega_0^2 \tag{9}$$

and where

ω_M $\gamma 4\pi M_s$,
γ gyromagnetic ratio (2.8 MHz/G),
V sphere volume,
K (loop diameter)$^{-1}$,
$4\pi M_s$ saturation magnetization (1750 G for pure YIG).

The saturation magnetization and resonator unloaded Q, Q_u are related to the sphere linewidth and magnetic biasing field H_0 by the expression [11]

$$Q_u = \frac{H_0 - \frac{1}{3}4\pi M_s}{\Delta H}. \tag{10}$$

The resonant frequency is linearly related to the magnetic biasing field according to the expression

$$f_0 = \gamma H_0. \tag{11}$$

Equations (8) and (9) show that both the equivalent inductance and capacitance of the resonator are functions of frequency and, therefore, functions of magnetic biasing field and tuning current. The two reactive degrees of freedom are factors in the usefulness of YIG devices as

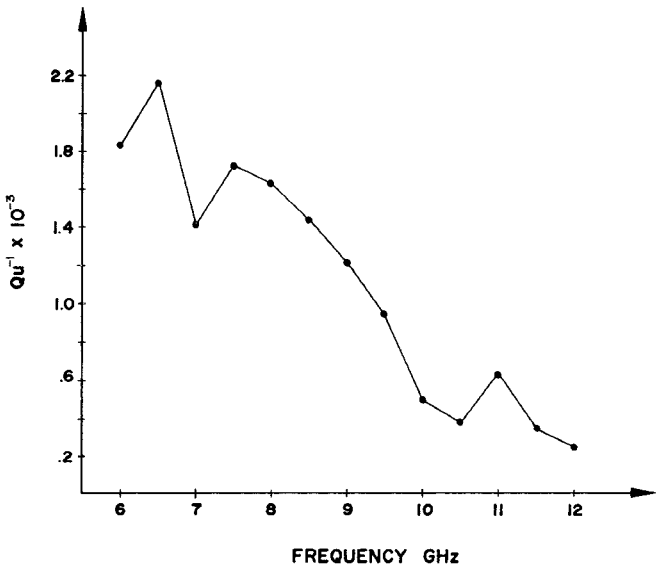

Fig. 2. Inverse unloaded Q for a YIG resonator.

high-Q, multioctave, and linear tuning elements. Equation (7) shows that the real part of the resonator input admittance is dependent upon material parameters and the geometry of the sphere and coupling structure. The conductance is an inverse function of the resonator unloaded Q which varies according to (10) and increases with frequency. The resonator conductance, therefore, decreases with frequency as illustrated in the measured Q_u results shown in Fig. 2 for an X-band YIG resonator. According to (2) the decreasing resonator conductance at higher frequencies indicates that the resonator can support oscillations for active devices with decreasing negative conductances at the high end of their operating bands. Due to this behavior, steady-state oscillations are possible with YIG-tuned oscillators when the resonator is presented with a negative conductance of relatively small magnitude. This behavior results in broad-band operation for YIG-tuned oscillators.

IV. Feedback Circuit Design

In order to generate a negative conductance over the frequency range of interest, various feedback circuit topologies and element values are considered. For YIG-tuned oscillators it is desirable that an inductive admittance be presented to the resonator in order to avoid spurious oscillations with the inductive coupling loop. This requirement limits the possible circuit configurations to those similar to the one shown in Fig. 1. A common gate configuration is normally employed with a common lead inductor used as the negative conductance generating phase-shift element. The admittance presented to the resonator by such a circuit is shown in Fig. 3. Decreasing the value of the feedback inductor L_f decreases the magnitude of the negative conductance but shifts the negative conductance bandwidth to higher frequencies. This feedback configuration does not generate a negative conductance

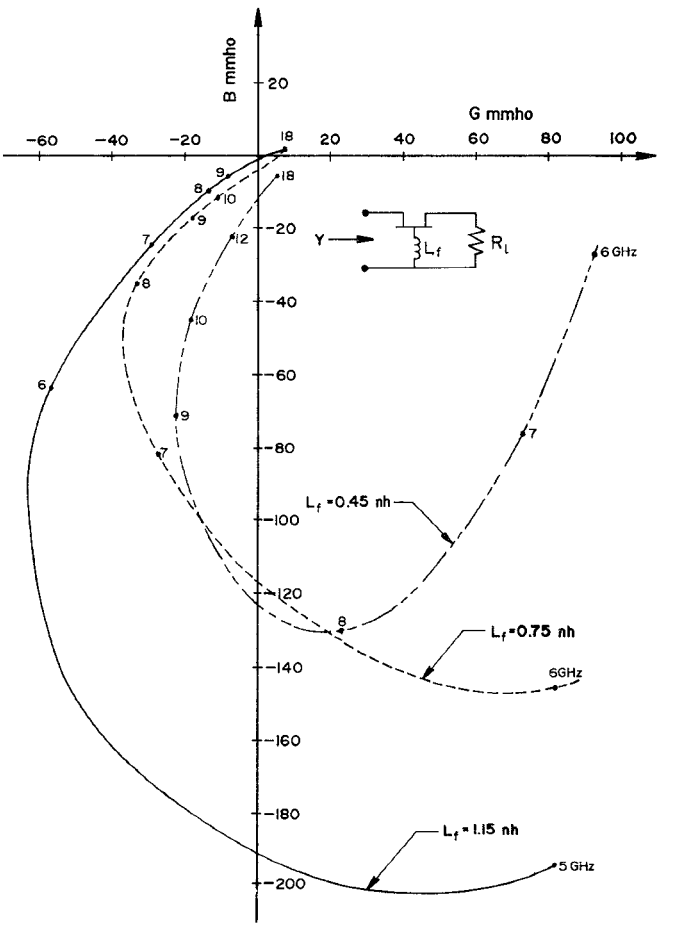

Fig. 3. Admittance of the active circuit for various gate feedback inductors.

above 15 GHz for the device used (i.e., the 1-micron gate length, 500-micron gate width device manufactured by the Hewlett–Packard Company) for any value of feedback inductance. The feedback inductor alone is not able to provide feedback to generate a negative conductance over an octave bandwidth.

In order to enhance the bandwidth and negative conductance magnitude, additional feedback elements are required. For example, it has been shown [12] that an additional inductive feedback element between the drain and source extends the operating bandwidth of the oscillator to more than an octave. The additional feedback can also be provided by the circuit presented to the drain of the FET. Fig. 4 shows a mapping of the admittance presented to the resonator (i.e., Y_d in Fig. 1) at a fixed frequency for a device and feedback circuit in which all possible passive loads are presented to the drain terminal of the FET. Greater than 50-Ω loads result in a decrease in negative conductance. Loads less than 50 Ω, however, result in an enhanced negative conductance. More enhancement is obtained from inductive than capacitive loads. Loads approaching an open circuit result in improper phase shift, and the conductance becomes positive.

The influence of the drain load upon Y_d can be determined from

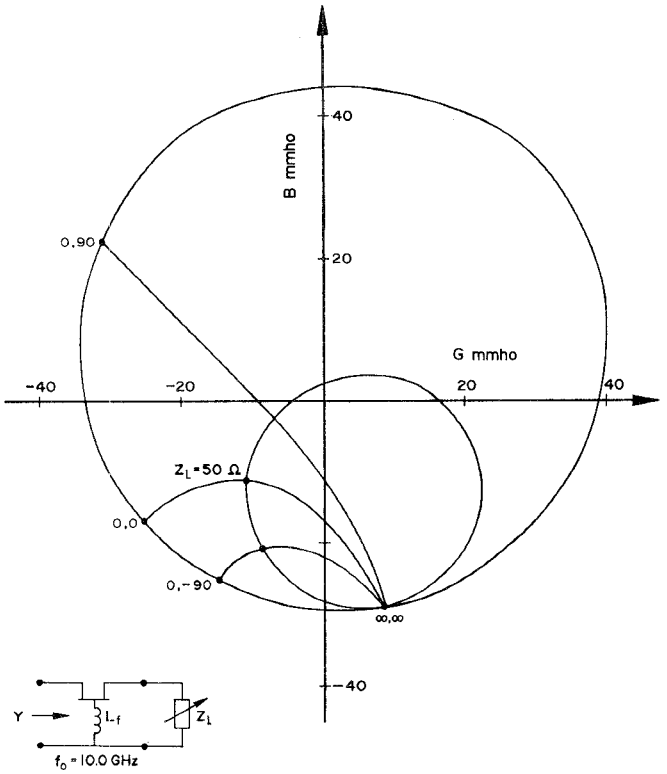

Fig. 4. Admittance of the active circuit as a function of the drain circuit load ($f_0 = 10.0$ GHz, $L_f = 0.65$ nH; the points labelled $Z_L = 50\ \Omega$; 0, 0; 0, 90; etc.; refer to $Z_L = 50 + j0\ \Omega$; $Z_L = 0 + j0\ \Omega$; $Z_L = 0 + j50\ \Omega$; etc.).

$$Y_d = Y_0\left[\frac{1 - S'_{11}}{1 + S'_{11}}\right] \tag{12}$$

where Y_0 has its standard meaning and S'_{11} is the resultant S_{11} when the load with reflection coefficient Γ_l is connected to the load or S_{22}-port of the FET and inductive feedback two-port (Fig. 1). The value of S'_{11} can be determined from

$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_l}{1 - S_{22}\Gamma_l}. \tag{13}$$

Since the S_{11} of the FET and gate feedback circuit represents a negative conductance over a certain frequency range, it is desirable to design the load circuit so that Γ_l provides feedback that adds in phase with that of S_{11}. This can be accomplished by defining an ideal drain circuit reflection coefficient. To do this set

$$\frac{S_{12}S_{21}\Gamma_l}{1 - S_{22}\Gamma_l} = \frac{1}{S^*_{11}} \tag{14}$$

and define

$$\Gamma_{l_{\text{ideal}}} = \frac{1}{S^*_{11}S_{12}S_{21} + S_{22}}. \tag{15}$$

A plot of $\Gamma_{l_{\text{ideal}}}$ is shown by the solid line in Fig. 5 for a circuit designed to operate from 8 to 12 GHz. The shape of the $\Gamma_{l_{\text{ideal}}}$ curve suggests a filter circuit since it is desirable to have a low magnitude reflection coefficient in midband with feedback provided by the increasing reflection coefficient at the band edges. Low-pass, high-pass, and bandpass filter designs all have been found to work, although high-pass filters have been found to work best. Although it is possible to synthesize circuits that more closely approximate the ideal drain circuit of Fig. 5, a constant-k filter design (Fig. 6) is adequate to enhance the negative conductance over the design range. The filter element values are selected according to the expressions

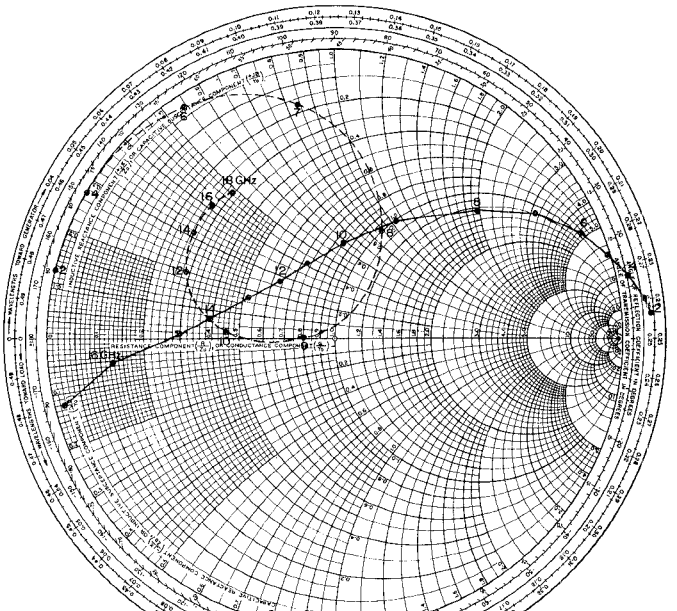

Fig. 5. Ideal and actual drain filter reflection coefficients (——$\Gamma_{l_{\text{ideal}}}$, – – – –$\Gamma_{l_{\text{actual}}}$).

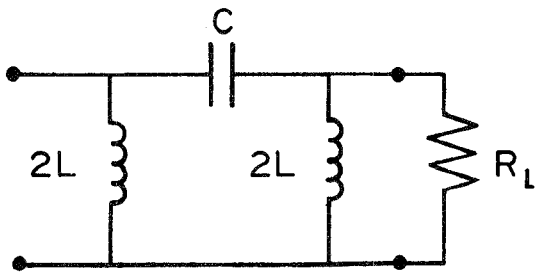

Fig. 6. FET oscillator drain filter circuit.

$$R = \sqrt{L/C} \tag{16}$$

and

$$f_c = 1/4\pi\sqrt{LC}. \tag{17}$$

Therefore,

$$C = 1/4\pi f_c R \tag{18}$$

and

$$L = R/4\pi f_c. \tag{19}$$

In practice, the gate feedback inductor is selected to produce a negative conductance at the high end of the desired frequency range, and the low-frequency end is

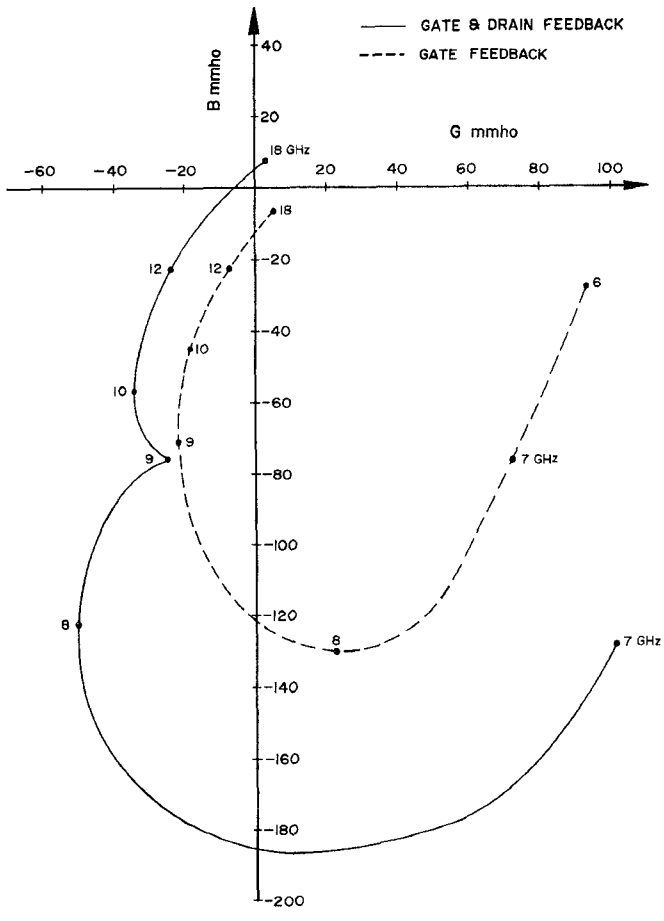

Fig. 7. Active circuit admittance for an X-band FET oscillator.

provided by feedback from the drain filter. In this manner, the negative conductance bandwidth can be extended to greater than octave coverage. The impedance R of the filter can be adjusted to maximize the magnitude of the negative conductance. The broken line in Fig. 5 shows the reflection coefficient of a filter designed with an impedance of 20 Ω. The cutoff frequency f_c has been set equal to the lower frequency of the desired frequency band, in this case 8 GHz, so that the filter feedback adds in phase to S_{11}. The admittance presented to the resonator by the complete oscillator circuit is shown in Fig. 7 by the solid line. Also shown for comparison is the admittance developed by the oscillator circuit with only gate inductor feedback. The enhancement of both bandwidth and the magnitude of the negative conductance is clearly evident.

A resonance at 9 GHz is just beginning to develop in the admittance curve of Fig. 7. The occurrence of the resonance is related to the impedance level of the drain filter circuit. As the impedance level is lowered the resonance grows and can result in multiple frequency operation and, ultimately, the midband portion of the admittance characteristic obtaining positive conductance values. Oscillations, of course, cease over this portion of the frequency band. This condition can be corrected by increasing the impedance level of the filter and accepting a slight reduction in bandwidth and negative conductance.

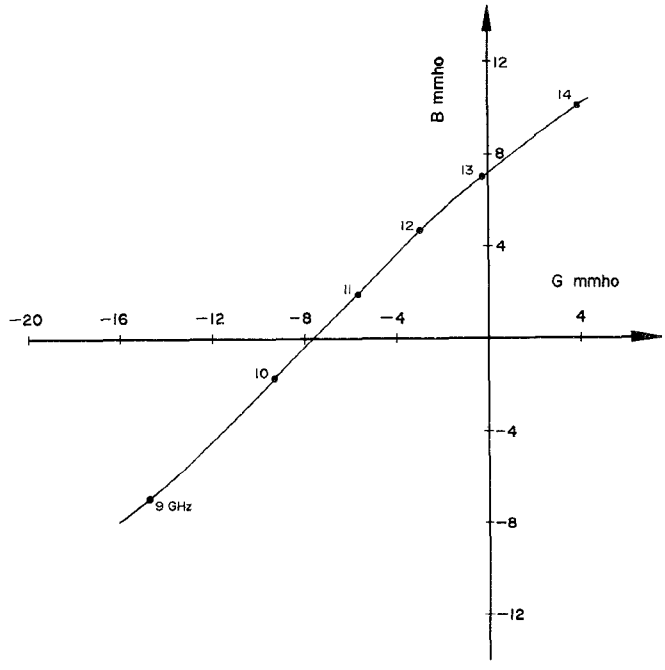

Fig. 8. Active circuit admittance showing spurious oscillation potential.

V. Spurious Oscillations

Careful circuit layout is required in order to prevent spurious oscillations from occurring at the high end of the frequency band. The possibility of spurious oscillations exists when Y_d shifts from an inductive to capacitive susceptance while maintaining a negative conductance as shown in Fig. 8. Under these circumstances, the oscillation conditions expressed in (1)–(4) can be satisfied, and an oscillation results even with no YIG bias. Such oscillations have been experimentally observed and are termed spurious because they do not tune with the YIG resonator. The oscillation frequency is fixed for a given FET bias condition and can be changed by altering the length of the YIG sphere coupling loop. The active device and feedback circuit behave as a parallel resonant circuit which is shunted by the inductive YIG sphere coupling loop. An equivalent circuit that can be used to calculate the spurious oscillation frequency is shown in Fig. 9. The oscillation frequency is calculated and plotted in Fig. 10.

In order to eliminate the possibility of spurious oscillations, care is required in both the active circuit and resonator design. The inductance of the coupling loop should be minimized so that the spurious oscillation frequency occurs out of the negative conductance region. The gate feedback inductor should be kept as small as possible because the value of this element is inversely proportional to the frequency at which the change from inductive to capacitive susceptance occurs. Parasitic reactances must also be minimized, especially parasitic capacitances. Fig. 11 illustrates the effect of parasitic source-to-ground capacitance upon Y_d. The parasitic capacitance does not change the relative negative conductance bandwidth, but it causes a capacitive shift of the entire admit-

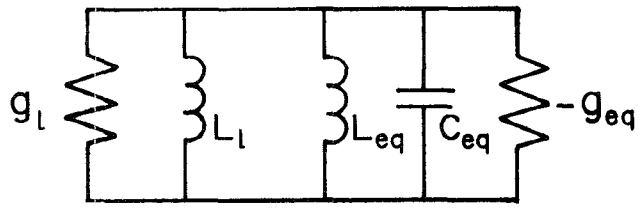

Fig. 9. Equivalent circuit for calculating spurious oscillation frequency (subscript L refers to YIG resonator coupling loop, subscript eq indicates equivalent lumped parameters calculated from Y_d at resonance).

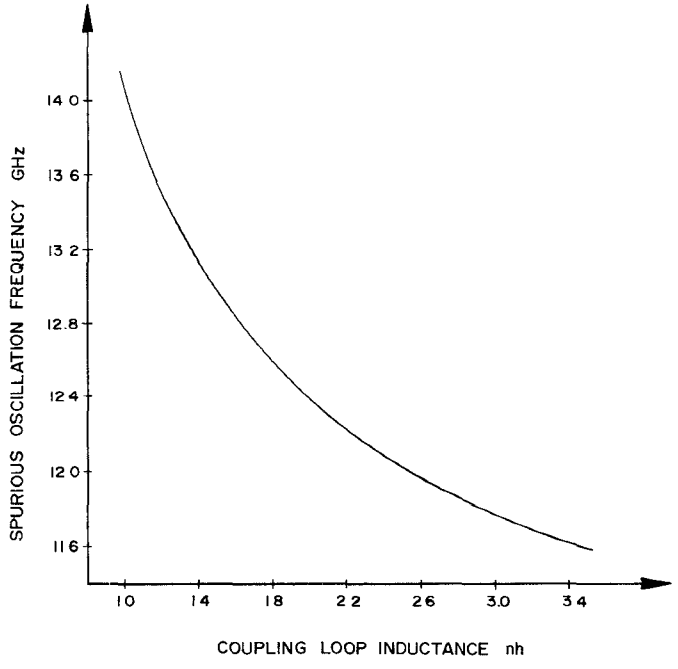

Fig. 10. Spurious oscillation frequency versus YIG coupling loop inductance.

tance curve. Parasitic source-to-ground capacitance is usually present in YIG tuned oscillators due to the mechanical support required for the coupling loop structure of the resonator. Since a capacitance of 0.05 pF is sufficient to cause a potential spurious oscillation problem (Fig. 11), support pads must be kept as small as is physically practical.

VI. Experimental Results

Using the design techniques discussed in this paper and utilizing thin-film MIC technology, an oscillator was designed to operate over the X-band frequency range of 8–12 GHz. A short-circuited transmission line with a calculated characteristic impedance of 200 Ω was used as the gate feedback element. The drain filter was constructed with a 0.5-pF chip capacitor and two short-circuited 100-Ω transmission lines. Adjustments in the operation of the oscillator are possible by using short-circuited bond wires to alter the length of the inductive elements. The characteristic impedance of the filter was designed to be 25 Ω which was sufficient to avoid the midband resonance appearing in Fig. 7. The circuit and

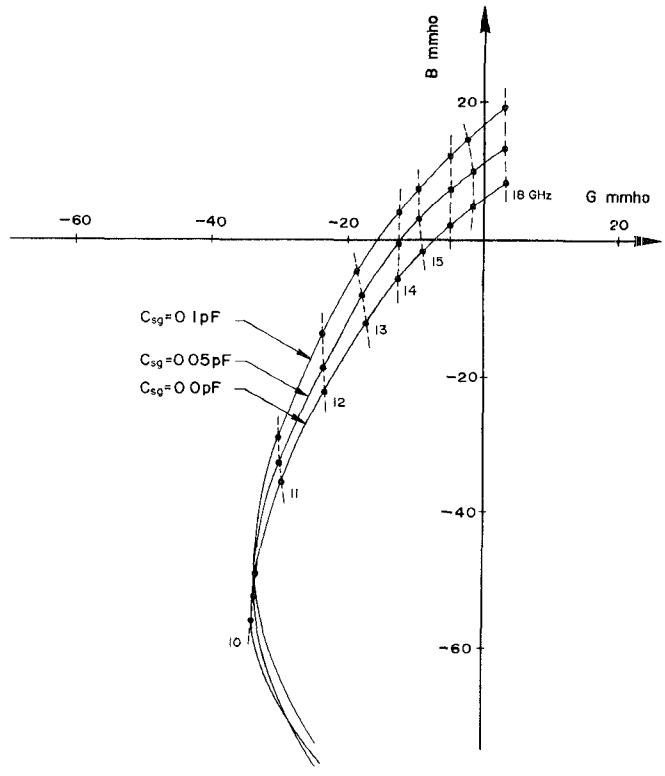

Fig. 11. Effect of parasitic source-to-ground capacitance on the active circuit admittance.

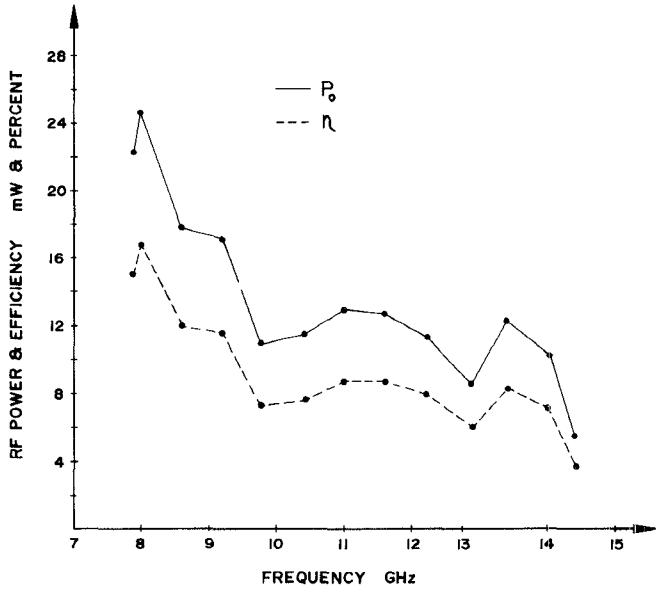

Fig. 12. Oscillator RF power/frequency performance.

unpackaged FET chip were assembled on a BeO ceramic to provide good heat-sinking properties.

The power versus frequency characteristic obtained from the oscillator is shown in Fig. 12. The oscillator operated from 7.9 to 14.4 GHz which is in excellent agreement with the predicted response. Approximately 10-mW minimum RF power was obtained from 7.9 to 14 GHz with a peak RF power of 25 mW at 8 GHz. The conversion efficiency was greater than 6 percent from 7.9

to 14 GHz and had a peak value of 17 percent at 8 GHz. No spurious oscillations were present during the operation of the oscillator.

VII. Conclusions

Design techniques that have been successfully used on the development of an X-band YIG-tuned FET oscillator have been presented. The design involves an investigation of the interface between the microwave resonator and device and feedback circuit. Small-signal device characterization is utilized and is found to result in excellent agreement between the computer bandwidth predictions and experimental results. The design technique results in maximization of the oscillator bandwidth. Potential resonance and spurious oscillation problems have been discussed and methods for their elimination presented.

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A Fast Low-Loss Microstrip p-i-n Phase Shifter

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***Abstract*—A 4-bit p-i-n phase shifter with low RF attentuation, fast switching time, and low switching power requirements is described. The circuit, made in microstripline, consists of four cells giving phase shifts of 180, 90, 45, and 22.5°, respectively. Each cell consists of a 3-dB coupler loaded by two p-i-n diodes. The transmission loss is 1.6 dB ±0.2 dB over the operating bandwidth of 11.7–12.2 GHz for a biasing current of only 5 mA/cell. Switching time between phase states is 1 ns.**

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I. Introduction

A PHASE SHIFTER has been developed at 12 GHz which has faster switching time, lower switching current requirement, and lower RF transmission loss than phase shifters previously reported at this frequency [1]–[3]. This phase shifter looks attractive for use in phased arrays for airborne and space applications [4]. These utilizations impose severe constraints on the phase shifter in terms of switching power dissipation and switching time duration. To fulfill these requirements, circuit design and diode

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